REMARKS

By this amendment, Claims 11, 12, 24 and 29 have been amended and new Claims 35-67 have been added. Hence, Claims 1-67 are pending in this application. The amendments to the claims and the new claims do not add any new matter to this application. All issues raised in the Office Action mailed February 9, 2001 are addressed hereinafter.

OBJECTION TO DRAWINGS

The drawings have been objected to on the ground that FIGS. 1A, 1B, 2, 3A and 3B should be designated by a legend such as "Prior Art" on the basis that only that which is old is illustrated in these figures. A request for approval of drawing amendment under 37 C.F.R. § 1.121 is submitted herewith for consideration by the Examiner. The proposed amendment adds the legend "Prior Art" to FIGS. 1A, 1B, 2, 3A and 3B.

OBJECTION TO CLAIMS 24 AND 29

Claims 24 and 29 have been objected to on the ground that the gerund (ing) form of verbs should be used. Method Claim 24 has been amended to change the verbs to the "ing" form as requested by the Examiner. Apparatus Claim 29 has not been amended at this time, however, because Applicant respectfully submits that the current claim language of "a routing mechanism configured to...determine...determine...and update..." is grammatically preferable to "a routing mechanism configured to...determining...determining...and updating..." Reconsideration and withdrawal of

the objection to Claims 24 and 29 in view of the amendment to Claim 24 and the foregoing comments with respect to Claim 29 is respectfully requested.

REJECTION OF CLAIM 12 UNDER 35 U.S.C. §112, SECOND PARAGRAPH

Claim 12 was rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. The stated basis for this rejection is that the claim language "routing the routing path" is unclear and the Examiner has kindly suggested "routing the path" as a preferable alternative. Claim 12 has been amended to recite "...provide additional space for the routing path..." which Applicant believes addresses the concerns raised by the Examiner. Accordingly, reconsideration and withdrawal of the rejection of Claim 12 under 35 U.S.C. §112, second paragraph is respectfully requested. Claim 11 has been amended to address the same issue.

REJECTION OF CLAIMS 1-6, 10-20, 22 AND 24-34 UNDER 35 U.S.C. §103(a)

Claims 1-6, 10-20, 22 and 24-34 were rejected under 35 U.S.C. §103(a) as being unpatentable over *An Interactive Router for Analog IC Design*, by Thorsten Adler and Jurgen Scheible ("*Adler*"). It is respectfully submitted that Claims 1-6, 10-20, 22 and 24-34 are patentable over *Adler* for at least the reasons provided hereinafter.

CLAIM 1

Claim 1 recites a method for automatically routing an integrated circuit that requires the steps of:

> "receiving integrated circuit layout data that defines a set of two or more integrated circuit devices to be included in the integrated circuit;

receiving integrated circuit connection data that specifies one or more electrical connections to be made between the integrated circuit devices;

determining, based upon the integrated circuit layout data and the integrated circuit connection data, a set of one or more routing indicators that specify a set of one or more preferable intermediate routing locations through which a routing path is to be located to connect first and second integrated circuit devices from the set of two or more integrated circuit devices;

determining, based upon the integrated circuit layout data, the integrated circuit connection data and the set of one or more routing indicators, the routing path between the first and second integrated circuit devices, wherein the routing path satisfies specified design criteria; and

updating the integrated circuit layout data to generate updated integrated circuit layout data that reflects the routing path between the first and second integrated circuit devices."

Claim 1 addresses the problem of how to automatically route an integrated circuit while avoiding problems appurtenant to conventional automated routing approaches.

Adler discloses an interactive analog IC design tool that uses an Analog Router (AR) and a Global Router (GR). The AR is implemented by a single layer maze router with a special oversizing algorithm and advanced treatment of arbitrary polygons. The oversizing algorithm enables placement of diagonal path segments near obstacle corners to increase layout density.

It is respectfully submitted that *Adler* does not in any way teach or suggest at least several of the steps required by Claim 1. For example, Claim 1 requires the step of "determining, based upon the integrated circuit layout data and the integrated circuit connection data, **a set of one or more routing indicators that specify a set of one or more preferable intermediate routing locations through which a routing path is to be located** to connect first and second integrated circuit devices from the set of two or more integrated circuit devices." Claim 1 also requires the step of "determining, based upon the integrated circuit layout data, the integrated circuit connection data and the set

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of one or more routing indicators, the routing path between the first and second integrated circuit devices, wherein the routing path satisfies specified design criteria." Neither of these required steps is in any way taught or suggested by *Adler*. In *Adler*, there is no determination of intermediate routing locations or points of any kind through which a routing path is to be located. The tool of *Adler* uses a wavefront search with a cost function to determine a general routing path from a source to a destination with the lowest cost. The wavefront search examines all points on the plane, leading outward from the starting point. During global routing, the GR generates tunnel polygons that define the area (grid points) in which the final routing can be performed by the AR. The tunnel polygons of *Adler* are similar to the fences of *Arnold* in that they define boundaries of areas within which final routing may occur. Hence, neither the wavefront search nor the use of tunnel polygons is in any way related to specifying "a set of one or more preferable intermediate routing locations through which a routing path is to be located," as required by Claim 1.

Section 3.1 of *Adler* describes the use of a two-dimensional bitmap in the database of the GR that stores information about the layout grid. Each grid point has an associated 32 bit integer value that stores information about the grid point. In particular, "bits 21 to 29 store information whether it's forbidden to extend the wave from the current grid point to the neighboring grid points." Referring to the example in Figure 6, bits 21 to 29 of the integer value associated with grid point *a* are set to indicate that the wave cannot be propagated from point *a* into grid points *b*, *c*, *d*, *e* or *f*. Thus, the integer values specify directions where the wavefront search cannot be propagated and do not indicate locations through which a routing path is to be located. In the example in Figure

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6, the integer value associated with grid point *a* does not indicate whether the routing path is to be located from grid point *a* to the grid point to the left, down, or down and left of grid point *a*, even though all three are available choices. Thus, the integer values associated with grid points maintained in the database of the GR do not in any way teach or suggest the step of "determining...a set of one or more preferable intermediate routing locations through which a routing path is to be located," as required by Claim 1.

For at least these reasons, it is respectfully submitted that Claim 1 is not in any way taught or suggested by *Adler* and that Claim 1 is therefore patentable over *Adler*.

CLAIMS 2-6 AND 10-20

Claims 2-6 and 10-20 depend from Claim 1 and include all of the limitations of Claim 1. Accordingly, it is respectfully submitted that Claims 2-6 and 10-20 are patentable over *Adler* for at least the reasons provided herein with respect to Claim 1. Furthermore, it is respectfully submitted that Claims 2-6 and 10-20 recite additional limitations that independently render them patentable over *Adler*.

For example, Claim 2 requires the additional step of:

"wherein determining the routing path includes determining, based upon the integrated circuit layout data, the integrated circuit connection data, bias direction criteria and straying limit criteria, the routing path between the first and second integrated circuit devices, wherein the bias direction criteria specifies a preferred routing direction for a routing path between first and second integrated circuit devices from the set of two or more integrated circuit devices and the straying limit criteria defines a routing region in which the routing path between the first and second integrated circuit devices may be placed."

As previously described herein with respect to Claim 1, the tunnel polygons define a region within which final routing may occur and the integer values specify forbidden directions for propagating the wavefront search, but *Adler* does not in any way teach or suggest the use of bias direction criteria that specified a preferred routing

direction for a routing path. The Office Action indicates that the additional step required by Claim 2 is taught or suggested by the text in Section 3.4 of *Adler*. It is respectfully submitted that Section 3.4 of *Adler* does not in any way teach or suggest the use of bias direction criteria and the Examiner is invited to identify specific text or figures of *Adler* that in any way teach or suggest the use of bias direction criteria as is required by Claim 2. For at least these reasons, it is respectfully submitted that Claim 2 is not in any way taught or suggested by *Adler* and that Claim 2 is therefore patentable over *Adler*.

As another example, Claim 3 requires the additional steps of:

"identifying one or more obstacles that block the routing path,
determining, based upon the integrated circuit layout data, the integrated circuit connection data and the one or more obstacles, one or more additional routing indicators that specify one or more preferable routing locations through which the routing path is to be located to avoid the one or more obstacles, and
determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the one or more additional routing indicators, the routing path between the first and second integrated circuit devices."

Claim 3 addresses the problem of how to route an integrated circuit when the layout may contain obstacles. According to Claim 3, obstacle avoidance is performed by identifying obstacles that block the routing path and determining additional routing indicators that specify "preferable routing locations through which the routing path is to be located to avoid the one or more obstacles." The only mention of obstacle avoidance in *Adler* appears in the context of using a special sizing procedure for diagonal wires to satisfy distance rules. See, e.g., Sections 2.2.1 and 3.1. The Office Action indicates that the additional steps required by Claim 3 are taught or suggested by the text in Sections 3.1- 3.4 of *Adler*. After reviewing these portions of *Adler*, it is respectfully submitted that these portions of *Adler* only briefly mention obstacles and including a level in the

GR database for obstacle polygons, and that there are insufficient details to support the conclusion that the specific steps required by Claim 3 are taught or suggested by these portions of *Adler*. For at least these reasons, it is respectfully submitted that Claim 3 is not in any way taught or suggested by *Adler* and that Claim 3 is therefore patentable over *Adler*.

As yet another example, Claim 10 requires the additional steps of:

> "identifying one or more obstacles that block the routing path, and determining, based upon the integrated circuit layout data, the integrated circuit connection data and the set of one or more routing indicators, the routing path between the first and second integrated circuit devices, wherein the routing path is routed from the second integrated circuit device to the first integrated circuit device."

Claim 10 addresses the problem of how to route an integrated circuit when the layout may contain obstacles. According to Claim 10, obstacle avoidance is performed by routing from the second integrated circuit device to the first integrated circuit device. This approach is not in any way taught or suggested by *Adler*. Section 2.3 of *Adler* discloses "direction preserving backtracking from target to source and path generation is similar to Lee's algorithm." Conventional Lee algorithms use a wavefront search to identify a set of all possible routing paths from the source to the target. Backtracking is then used to select a path from the set of all possible routing paths that has the least cost. Thus, the backtracking described in *Adler* refers to backtracking over routes determined from the source to the target and there is no mention of routing from the target to the source to avoid obstacles.

The Office Action indicates that the additional steps required by Claim 10 are taught or suggested by the text in Sections 3.1 and 3.3 of *Adler*. Section 3.1 describes aspects of the GR database including the use of the two-dimensional bitmap and issues

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relating to overlapping polygons, and Section 3.3 describes path generation by the GR and AR. It is respectfully submitted that neither Section 3.1 nor Section 3.3 of *Adler* in any way teach or suggest avoiding obstacles by routing from the target to the source, as is required by Claim 10. The Examiner is invited to identify specific text or figures of *Adler* that in any way teach or suggest the steps required by Claim 10. For at least these reasons, it is respectfully submitted that Claim 10 is not in any way taught or suggested by *Adler* and is therefore patentable over *Adler*.

As a further example, Claim 16 requires the additional step of:

"performing one or more design rule checks on one or more portions of the routing path as the routing path is being determined."

Conventional layout synthesis tools normally provide some type of design rule checking to ensure that a layout satisfies a set of design rules. Design rule checking is conventionally performed as a separate phase in layout synthesis. Claim 16 requires "on-the-fly" design rule checking on one or more portions of the routing path "as the routing path is being determined." *Adler* describes design rule checking generally, but does not in any way teach or suggest the use of "on-the-fly" design rule checking as required by Claim 16. The Office Action indicates that the additional steps required by Claim 16 are taught or suggested by the Abstract, Figures 1 and 2 and Sections 2.1 – 2.2.2 of *Adler*. It is respectfully submitted that these portions of *Adler* teach or suggest design rule checking generally and not the "on-the-fly" design rule checking required by Claim 16. The Examiner is invited to identify any disclosure of *Adler* that in any way teaches or suggests the steps required by Claim 16. For at least these reasons, it is respectfully submitted that Claim 16 is not in any way taught or suggested by *Adler* and is therefore patentable over *Adler*.

CLAIM 22

Claim 22 recites a method for automatically routing an integrated circuit that requires the steps of:

> "receiving integrated circuit layout data that defines a set of two or more integrated circuit devices to be included in the integrated circuit;
> receiving integrated circuit connection data that specifies one or more electrical connections to be made between the integrated circuit devices;
> determining, based upon the integrated circuit layout data and the integrated circuit connection data, a set of two or more join points that are to be electrically connected, wherein each join point from the set of two or more join points has an associated set of specified design criteria that control attachment of routing paths thereto;
> determining, based upon the integrated circuit layout data and the set of two or more join points, one or more routing paths to connect the set of two or more join points, wherein the one or more routing paths satisfy the specified design criteria associated with the set of two or more join points; and
> updating the integrated circuit layout data to generate updated integrated circuit layout data that reflects the one or more routing paths."

Claim 22 recites an approach for automatically routing an integrated circuit that requires the use of join point-specific design criteria to control the attachment of routing paths to join points. Using join point-specific design criteria allows relatively greater flexibility than conventional approaches that use global design criteria. For example, using join point-specific design criteria allows design rules to be selectively applied to join points and not to, for example, routing paths, other layout features or other join points.

Adler discloses using a cost function to select a particular path from the source to target and does not in any way teach or suggest using join point-specific design criteria to automatically route an integrated circuit. The Office Action indicates that the approach recited in Claim 22 is taught or suggested by Sections 2.2 – 2.4 of *Adler*. These portions

of *Adler* discuss how a wire is connected to points on the source and target, but there is no mention of using a set of specified design criteria to control the attachment of the wire to these points on the source and target. The Examiner is invited to identify specific disclosure of *Adler* that in any way teaches or suggests the use of join points and associated specified design criteria to control attaching wires to the

For at least these reasons, it is respectfully submitted that Claim 22 is not in any way taught or suggested by *Adler* and is therefore patentable over *Adler*.

CLAIMS 24-34

Claims 24-28 are similar to Claims 1-5, except in the context of a computer-readable medium. Therefore, it is respectfully submitted that Claims 24-28 are patentable over *Adler* for at least the reasons set forth herein with respect to Claims 1-5. Claims 29-33 are similar to Claims 1-5, except in the context of a computer system. Therefore, it is respectfully submitted that Claims 29-33 are patentable over *Adler* for at least the reasons set forth herein with respect to Claims 1-5. Claim 34 depends from Claim 1 and includes all of the limitations of Claim 1. Accordingly, it is respectfully submitted that Claim 34 is patentable over *Adler* for at least the reasons provided herein with respect to Claim 1. Furthermore, it is respectfully submitted that Claim 34 recites additional limitations that independently render Claim 34 patentable over *Adler*.

In view of the foregoing, reconsideration and withdrawal of the rejection of Claims 1-6, 10-20, 22 and 24-34 under 35 U.S.C. §103(a) as being unpatentable over *Adler* is respectfully requested.

REJECTION OF CLAIMS 7-9 UNDER 35 U.S.C. §103(a)

Claims 7-9 were rejected under 35 U.S.C. §103(a) as being unpatentable over *Adler* and *Codar: A Congestion-Directed General Area Router*, by Ping-San Tzeng and Carlo H. Sequin ("*Tzeng*"). It is respectfully submitted that Claims 7-9 are patentable over *Adler* and *Tzeng*, alone or in combination, for at least the reasons provided hereinafter.

Claims 7-9 depend from Claim 1 and include all of the limitations of Claim 1. *Tzeng* is relied upon for its disclosure of rip-up and reroute techniques that are not taught or suggested by *Adler*. *Tzeng*, however, does not in any way teach or suggest an approach for automatically routing and integrated circuit using routing indicators that "specify a set of one or more preferable intermediate routing locations through which a routing path is to be located" as is required by Claims 7-9.

Accordingly, for this reason and the reasons set forth herein with respect to Claim 1, it is respectfully submitted that Claims 7-9 are not in any way taught or suggested by *Adler* and *Tzeng*, alone or in combination. Reconsideration and withdrawal of the rejection of Claims 7-9 under 35 U.S.C. §103(a) as being unpatentable over *Adler* and *Tzeng* is therefore respectfully requested.

REJECTION OF CLAIM 21 UNDER 35 U.S.C. §103(a)

Claim 21 was rejected under 35 U.S.C. §102(a) as being unpatentable over *A Practical Online Design Rule Checking System*, by Goro Suzuki and Yoshio Okamura ("*Suzuki*"). It is respectfully submitted that Claim 21 is patentable over by *Suzuki* for at least the reasons provided hereinafter.

Claim 21 recites a method for automatically verifying an integrated circuit layout that requires the steps of:

> "receiving integrated circuit layout data that defines a set of two or more layout objects contained in the integrated circuit layout;
> performing a first design rule check on a layout object from the set of two or more layout objects by evaluating the layout object against specified design criteria;
> changing one or more values defined by the specified design criteria to generate updated specified design criteria, wherein the changing of the one or more values is performed after a specified amount of time has elapsed and is made with respect to either the layout object or one or more other layout objects from the set of two or more layout objects; and
> performing a second design rule check on the layout object by evaluating the layout object against the updated specified design criteria."

Claim 21 recites a time-varying design rule check approach for verifying an integrated circuit layout. One or more values defined by specified design criteria used for a design rule check are varied over time with respect to one or more layout objects contained in the integrated circuit layout. *Suzuki* discloses a conventional incremental design rule checking system that selectively applies all or a portion of a set of design rule checks to portions of an integrated circuit layout. While it is true, as set forth in the Office Action, that the incremental design rule checks in *Suzuki* may be performed repeatedly, *Suzuki* does not in any way teach or suggest selectively changing one or more values defined by the specified design criteria over time with respect to only one or more layout objects and using the changed values in a subsequent design rule check. It is therefore respectfully submitted that Claim 21 is not in any way taught or suggested by *Suzuki* and is therefore patentable over *Suzuki*. Accordingly, reconsideration and withdrawal of the rejection of Claim 21 under 35 U.S.C. §103(a) as being unpatentable over *Suzuki* is respectfully requested.

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REJECTION OF CLAIM 23 UNDER 35 U.S.C. §103(a)

Claim 23 was rejected under 35 U.S.C. §103(a) as being unpatentable over *Xiong*, U.S. Patent No. 5,550,748. It is respectfully submitted that Claim 23 is patentable over by *Xiong* for at least the reasons provided hereinafter.

Claims 23 recites a method for automatically routing an integrated circuit that requires the steps of:

> "receiving integrated circuit layout data that defines a set of two or more integrated circuit devices to be included in the integrated circuit;
> receiving integrated circuit connection data that specifies one or more electrical connections to be made between the integrated circuit devices;
> determining, based upon the integrated circuit layout data and the integrated circuit connection data, a routing path between first and second integrated circuit devices that satisfies specified design criteria, wherein determining the routing path between the first and second integrated circuit devices includes
> determining whether the distance to be routed for a portion of the routing path exceeds a specified distance, and
> if the distance to be routed for the portion of the routing path does not exceed the specified distance, then routing the portion of the routing path in a single step; and
> updating the integrated circuit layout data to generate updated integrated circuit layout data that reflects the routing path between the first and second integrated circuit devices."

The approach for automatically routing an integrated circuit recited in Claim 23 requires that a portion of a routing path be extended in a single step by an amount that does not exceed a specified distance. This approach is particularly useful in tight routing situations where the distance to be routed is so short that independent bends cannot be made, the selection of connection locales impacts the feasibility of routing or the remaining unrouted stretch after moving out from a join point is too short to add bends. In addition, construction of an entire feasible route in a single step allows error recovery

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mechanisms to make better decisions as to what should be removed. Otherwise, the recovery mechanism may have only short routing stubs as guidance.

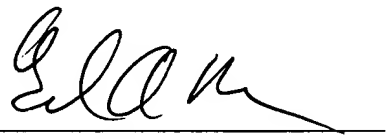
Xiong describes an approach for routing and integrated circuit layout that ensures that time delay constraints are satisfied. A search region is defined that satisfies specified time delay constraints. Connections are then routed to available locations within the search region. More specifically, *Xiong* teaches selecting the shortest delay path from a source pin of the signal net passing through a free point to a sink pin of the signal net and then routing the signal net along a routed path that includes the shortest delay path. *Xiong* does not in any way teach or suggest the steps required by Claim 23, namely "determining whether the distance to be routed for a portion of the routing path exceeds a specified distance, and if the distance to be routed for the portion of the routing path does not exceed the specified distance, then routing the portion of the routing path in a single step." The portions of *Xiong* identified in the Office Action do not in any way teach or suggest these steps. For at least these reasons, it is respectfully submitted that Claim 23 is patentable over *Xiong* and is therefore patentable over *Xiong*. Accordingly, reconsideration and withdrawal of the rejection of Claim 23 under 35 U.S.C. §103(a) as being unpatentable over *Xiong* is respectfully requested.

For the reasons set forth herein, it is respectfully submitted that all of the pending claims are in condition for allowance and the issuance of a notice of allowance is respectfully requested.

If there are any additional charges, please charge them to Deposit Account No. 50-1302.

Respectfully submitted,

HICKMAN PALERMO TRUONG & BECKER LLP



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on April 18, 2001 by Tirena Say
Tirena Say

MARKED UP VERSIONS OF CLAIMS

1. (NOT AMENDED) A method for automatically routing an integrated circuit, the method comprising the computer-implemented steps of:

receiving integrated circuit layout data that defines a set of two or more integrated circuit devices to be included in the integrated circuit;

receiving integrated circuit connection data that specifies one or more electrical connections to be made between the integrated circuit devices;

determining, based upon the integrated circuit layout data and the integrated circuit connection data, a set of one or more routing indicators that specify a set of one or more preferable intermediate routing locations through which a routing path is to be located to connect first and second integrated circuit devices from the set of two or more integrated circuit devices;

determining, based upon the integrated circuit layout data, the integrated circuit connection data and the set of one or more routing indicators, the routing path between the first and second integrated circuit devices, wherein the routing path satisfies specified design criteria; and

updating the integrated circuit layout data to generate updated integrated circuit layout data that reflects the routing path between the first and second integrated circuit devices.

2. (NOT AMENDED) The method as recited in Claim 1, wherein determining the routing path includes determining, based upon the integrated circuit layout data, the integrated circuit connection data, bias direction criteria and straying limit criteria, the routing path between the first and second integrated circuit devices, wherein the bias direction criteria specifies a preferred routing direction for a

routing path between first and second integrated circuit devices from the set of two or more integrated circuit devices and the straying limit criteria defines a routing region in which the routing path between the first and second integrated circuit devices may be placed.

3. (NOT AMENDED) The method as recited in Claim 1, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

determining, based upon the integrated circuit layout data, the integrated circuit connection data and the one or more obstacles, one or more additional routing indicators that specify one or more preferable routing locations through which the routing path is to be located to avoid the one or more obstacles, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the one or more additional routing indicators, the routing path between the first and second integrated circuit devices.

4. (NOT AMENDED) The method as recited in Claim 1, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

changing specified straying limit criteria that defines a routing region in which the routing path between the first and second integrated circuit devices may be placed to generate changed specified straying limit criteria that defines a modified routing region, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the changed

specified straying limit criteria, the routing path between the first and second integrated circuit devices.

5. (NOT AMENDED) The method as recited in Claim 1, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

determining a set of one or more layer changes to allow the routing path to avoid the one more obstacles, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the set of one or more layer changes, the routing path between the first and second integrated circuit devices.

6. (NOT AMENDED) The method as recited in Claim 1, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

determining a set of one or more bends to be included in the routing path to avoid the one more obstacles, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the set of one or more bends, the routing path between the first and second integrated circuit devices.

7. (NOT AMENDED) The method as recited in Claim 1, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

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determining one or more portions of the routing path to be ripped up and rerouted, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the one or more portions of the routing path to be ripped up and rerouted, the routing path between the first and second integrated circuit devices.

8. (NOT AMENDED) The method as recited in Claim 7, wherein determining the routing path between the first and second integrated circuit devices further includes

determining one or more portions of one or more other routing paths to be ripped up and rerouted, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators, the one or more portions of the routing path to be ripped up and rerouted and the one or more portions of the one or more other routing paths to be ripped up and rerouted, the routing path between the first and second integrated circuit devices.

9. (NOT AMENDED) The method as recited in Claim 1, wherein determining the routing path between the first and second integrated circuit devices further includes

identifying one or more obstacles that block the routing path,

determining one or more portions of one or more other routing paths to be ripped up and rerouted, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the one or

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more portions of the one or more other routing paths to be ripped up and rerouted, the routing path between the first and second integrated circuit devices.

10. (NOT AMENDED) The method as recited in Claim 1, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data and the set of one or more routing indicators, the routing path between the first and second integrated circuit devices, wherein the routing path is routed from the second integrated circuit device to the first integrated circuit device.

11. (AMENDED) The method as recited in Claim 1, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

determining one or more locations to employ corner clipping to provide additional space for [routing] the routing path, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the one or more locations to employ corner clipping, the routing path between the first and second integrated circuit devices.

12. (AMENDED) The method as recited in Claim 1, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

determining one or more integrated circuit layout objects to be moved to provide additional space for [routing] the routing path, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and moving the one or more integrated circuit layout objects, the routing path between the first and second integrated circuit devices.

13. (NOT AMENDED) The method as recited in Claim 1, wherein determining the routing path between the first and second integrated circuit devices includes

examining data that indicates whether changes can be made to one or more layout objects defined by the integrated circuit layout data to accommodate the routing of the routing path, and

if the data indicates that changes can be made to the one or more layout objects defined by the integrated circuit layout data to accommodate the routing of the routing path, then

making one or more changes to the one or more layout objects defined by the integrated circuit layout data, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the one or more changes made to the one or more layout objects, the routing path between the first and second integrated circuit devices.

14. (NOT AMENDED) The method as recited in Claim 13, further comprising generating data that specifies the one or more changes made to the one or more layout objects.

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15. (NOT AMENDED) The method as recited in Claim 1, wherein determining the routing path between the first and second integrated circuit devices includes determining a set of one or more routing targets to which the routing path is to be routed, and
determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the set of one or more routing targets, the routing path between the first and second integrated circuit devices.

16. (NOT AMENDED) The method as recited in Claim 1, wherein determining the routing path between the first and second integrated circuit devices includes performing one or more design rule checks on one or more portions of the routing path as the routing path is being determined.

17. (NOT AMENDED) The method as recited in Claim 16, further comprising performing a design rule check on the updated integrated circuit layout data, wherein the design rule check does not check one or more layout objects previously checked during determination of the routing path.

18. (NOT AMENDED) The method as recited in Claim 1, wherein determining the routing path between the first and second integrated circuit devices includes extending the routing path a specified amount to generate an extended portion of the routing path, and
selectively performing a design rule check on only the extended portion of the routing path.

19. (NOT AMENDED) The method as recited in Claim 1, wherein all attachment and bend angles defined by the updated integrated circuit layout data are multiples of ninety degrees.

20. (NOT AMENDED) The method as recited in Claim 1, wherein one or more attachment or bend angles defined by the updated integrated circuit layout data are multiples of other than ninety degrees.

21. (NOT AMENDED) A method for automatically verifying an integrated circuit layout, the method comprising the computer-implemented steps of:

receiving integrated circuit layout data that defines a set of two or more layout objects contained in the integrated circuit layout;

performing a first design rule check on a layout object from the set of two or more layout objects by evaluating the layout object against specified design criteria;

changing one or more values defined by the specified design criteria to generate updated specified design criteria, wherein the changing of the one or more values is performed after a specified amount of time has elapsed and is made with respect to either the layout object or one or more other layout objects from the set of two or more layout objects; and

performing a second design rule check on the layout object by evaluating the layout object against the updated specified design criteria.

22. (NOT AMENDED) A method for automatically routing an integrated circuit, the method comprising the computer-implemented steps of:

receiving integrated circuit layout data that defines a set of two or more integrated circuit devices to be included in the integrated circuit;

receiving integrated circuit connection data that specifies one or more electrical connections to be made between the integrated circuit devices;

determining, based upon the integrated circuit layout data and the integrated circuit connection data, a set of two or more join points that are to be electrically connected, wherein each join point from the set of two or more join points has an associated set of specified design criteria that control attachment of routing paths thereto;

determining, based upon the integrated circuit layout data and the set of two or more join points, one or more routing paths to connect the set of two or more join points, wherein the one or more routing paths satisfy the specified design criteria associated with the set of two or more join points; and

updating the integrated circuit layout data to generate updated integrated circuit layout data that reflects the one or more routing paths.

23. (NOT AMENDED) A method for automatically routing an integrated circuit, the method comprising the computer-implemented steps of:

receiving integrated circuit layout data that defines a set of two or more integrated circuit devices to be included in the integrated circuit;

receiving integrated circuit connection data that specifies one or more electrical connections to be made between the integrated circuit devices;

determining, based upon the integrated circuit layout data and the integrated circuit connection data, a routing path between first and second integrated circuit devices that satisfies specified design criteria, wherein determining the routing path between the first and second integrated circuit devices includes

determining whether the distance to be routed for a portion of the routing path exceeds a specified distance, and

if the distance to be routed for the portion of the routing path does not exceed the specified distance, then routing the portion of the routing path in a single step; and

updating the integrated circuit layout data to generate updated integrated circuit layout data that reflects the routing path between the first and second integrated circuit devices.

24. (TWICE AMENDED) A computer-readable medium carrying one or more sequences of one or more instructions for automatically routing an integrated circuit, the one or more sequences of one or more instructions including instructions which, when executed by one or more processors, cause the one or more processors to perform the steps of:

[receive] receiving integrated circuit layout data that defines a set of two or more integrated circuit devices to be included in the integrated circuit;

[receive] receiving integrated circuit connection data that specifies one or more electrical connections to be made between the integrated circuit devices;

determining, based upon the integrated circuit layout data and the integrated circuit connection data, a set of one or more routing indicators that specify a set of one or more preferable intermediate routing locations through which a routing path is to be located to connect first and second integrated circuit devices from the set of two or more integrated circuit devices;

[determine,] determining, based upon the integrated circuit layout data, the integrated circuit connection data and the set of one or more routing indicators, the routing path between the first and second integrated circuit devices, wherein the routing path satisfies specified design criteria; and

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[update] updating the integrated circuit layout data to generate updated integrated circuit layout data that reflects the routing path between the first and second integrated circuit devices.

25. (NOT AMENDED) The computer-readable medium as recited in Claim 24, wherein determining the routing path includes determining, based upon the integrated circuit layout data, the integrated circuit connection data, bias direction criteria and straying limit criteria, the routing path between the first and second integrated circuit devices, wherein the bias direction criteria specifies a preferred routing direction for a routing path between first and second integrated circuit devices from the set of two or more integrated circuit devices and the straying limit criteria defines a routing region in which the routing path between the first and second integrated circuit devices may be placed.

26. (NOT AMENDED) The computer-readable medium as recited in Claim 24, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

determining, based upon the integrated circuit layout data, the integrated circuit connection data and the one or more obstacles, one or more additional routing indicators that specify one or more preferable routing locations through which the routing path is to be located to avoid the one or more obstacles, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the one or more additional routing indicators, the routing path between the first and second integrated circuit devices.

27. (NOT AMENDED) The computer-readable medium as recited in Claim 24, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

changing specified straying limit criteria that defines a routing region in which the routing path between the first and second integrated circuit devices may be placed to generate changed specified straying limit criteria that defines a modified routing region, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the changed specified straying limit criteria, the routing path between the first and second integrated circuit devices.

28. (NOT AMENDED) The computer-readable medium as recited in Claim 24, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

determining a set of one or more layer changes to allow the routing path to avoid the one more obstacles, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the set of one or more layer changes, the routing path between the first and second integrated circuit devices.

29. (TWICE AMENDED) A system for automatically routing an integrated circuit, the system comprising:

a data storage mechanism having stored therein

integrated circuit layout data that defines a set of two or more integrated circuit devices to be included in the integrated circuit, and

integrated circuit connection data that specifies one or more electrical connections to be made between the integrated circuit devices; and

a routing mechanism communicatively coupled to the data storage mechanism,

the routing mechanism being configured to

determine, based upon the integrated circuit layout data and the integrated circuit connection data, a set of one or more routing indicators that specify a set of one or more preferable intermediate routing locations through which a routing path is to be located to connect first and second integrated circuit devices from the set of two or more integrated circuit devices,

determine, based upon the integrated circuit layout data, the integrated circuit connection data and the set of one or more routing indicators, the routing path between the first and second integrated circuit devices, wherein the routing path satisfies specified design criteria, and

update the integrated circuit layout data to generate updated integrated circuit layout data that reflects the routing path between the first and second integrated circuit devices.

30. (NOT AMENDED) The system as recited in Claim 29, wherein the routing mechanism is further configured to determine the routing path by determining, based upon the integrated circuit layout data, the integrated circuit connection data, bias direction criteria and straying limit criteria, the routing path between the first and second integrated circuit devices, wherein the bias direction criteria

specifies a preferred routing direction for a routing path between first and second integrated circuit devices from the set of two or more integrated circuit devices and the straying limit criteria defines a routing region in which the routing path between the first and second integrated circuit devices may be placed.

31. (NOT AMENDED) The system as recited in Claim 29, wherein the routing mechanism is further configured to determine the routing path between the first and second integrated circuit devices by

identifying one or more obstacles that block the routing path,

determining, based upon the integrated circuit layout data, the integrated circuit connection data and the one or more obstacles, one or more additional routing indicators that specify one or more preferable routing locations through which the routing path is to be located to avoid the one or more obstacles, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the one or more additional routing indicators, the routing path between the first and second integrated circuit devices.

32. (NOT AMENDED) The system as recited in Claim 29, wherein the routing mechanism is further configured to determine the routing path between the first and second integrated circuit devices by

identifying one or more obstacles that block the routing path,

changing specified straying limit criteria that defines a routing region in which the routing path between the first and second integrated circuit devices may be placed to generate changed specified straying limit criteria that defines a modified routing region, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the changed specified straying limit criteria, the routing path between the first and second integrated circuit devices.

33. (NOT AMENDED) The system as recited in Claim 29, wherein routing mechanism is further configured to determine the routing path between the first and second integrated circuit devices by

identifying one or more obstacles that block the routing path,

determining a set of one or more layer changes to allow the routing path to avoid the one more obstacles, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the set of one or more layer changes, the routing path between the first and second integrated circuit devices.

34. (NOT AMENDED) The method as recited in Claim 1, wherein each routing indicator from the set of one or more routing indicators further specifies a routing direction for the routing path.

35. (NEW) The computer-readable medium as recited in Claim 24, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

determining a set of one or more bends to be included in the routing path to avoid the one more obstacles, and

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determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the set of one or more bends, the routing path between the first and second integrated circuit devices.

36. (NEW) The computer-readable medium as recited in Claim 24, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

determining one or more portions of the routing path to be ripped up and rerouted, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the one or more portions of the routing path to be ripped up and rerouted, the routing path between the first and second integrated circuit devices.

37. (NEW) The computer-readable medium as recited in Claim 36, wherein determining the routing path between the first and second integrated circuit devices further includes

determining one or more portions of one or more other routing paths to be ripped up and rerouted, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators, the one or more portions of the routing path to be ripped up and rerouted and the one or more portions of the one or more other routing paths to be ripped up and rerouted, the routing path between the first and second integrated circuit devices.

38. (NEW) The computer-readable medium as recited in Claim 24, wherein determining the routing path between the first and second integrated circuit devices further includes

identifying one or more obstacles that block the routing path,

determining one or more portions of one or more other routing paths to be ripped up and rerouted, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the one or more portions of the one or more other routing paths to be ripped up and rerouted, the routing path between the first and second integrated circuit devices.

39. (NEW) The computer-readable medium as recited in Claim 24, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data and the set of one or more routing indicators, the routing path between the first and second integrated circuit devices, wherein the routing path is routed from the second integrated circuit device to the first integrated circuit device.

40. (NEW) The computer-readable medium as recited in Claim 24, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

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determining one or more locations to employ corner clipping to provide additional space for the routing path, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the one or more locations to employ corner clipping, the routing path between the first and second integrated circuit devices.

41. (NEW) The computer-readable medium as recited in Claim 24, wherein

determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

determining one or more integrated circuit layout objects to be moved to provide additional space for the routing path, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and moving the one or more integrated circuit layout objects, the routing path between the first and second integrated circuit devices.

42. (NEW) The computer-readable medium as recited in Claim 24, wherein

determining the routing path between the first and second integrated circuit devices includes

examining data that indicates whether changes can be made to one or more layout objects defined by the integrated circuit layout data to accommodate the routing of the routing path, and

if the data indicates that changes can be made to the one or more layout objects defined by the integrated circuit layout data to accommodate the routing of the routing path, then

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making one or more changes to the one or more layout objects defined by the integrated circuit layout data, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the one or more changes made to the one or more layout objects, the routing path between the first and second integrated circuit devices.

43. (NEW) The computer-readable medium as recited in Claim 42, further comprising one or more additional instructions which, when executed by the one or more processors, cause the one or more processors to generate data that specifies the one or more changes made to the one or more layout objects.

44. (NEW) The computer-readable medium as recited in Claim 24, wherein determining the routing path between the first and second integrated circuit devices includes

determining a set of one or more routing targets to which the routing path is to be routed, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the set of one or more routing targets, the routing path between the first and second integrated circuit devices.

45. (NEW) The computer-readable medium as recited in Claim 24, wherein determining the routing path between the first and second integrated circuit devices includes performing one or more design rule checks on one or more portions of the routing path as the routing path is being determined.

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46. (NEW) The computer-readable medium as recited in Claim 45, further comprising one or more additional instructions which, when executed by the one or more processors, cause the one or more processors to perform a design rule check on the updated integrated circuit layout data, wherein the design rule check does not check one or more layout objects previously checked during determination of the routing path.

47. (NEW) The computer-readable medium as recited in Claim 24, wherein determining the routing path between the first and second integrated circuit devices includes
extending the routing path a specified amount to generate an extended portion of the routing path, and
selectively performing a design rule check on only the extended portion of the routing path.

48. (NEW) The computer-readable medium as recited in Claim 24, wherein all attachment and bend angles defined by the updated integrated circuit layout data are multiples of ninety degrees.

49. (NEW) The computer-readable medium as recited in Claim 24, wherein one or more attachment or bend angles defined by the updated integrated circuit layout data are multiples of other than ninety degrees.

50. (NEW) A computer-readable medium carrying one or more sequences of one or more instructions for automatically verifying an integrated circuit layout, the one or more sequences of one or more instructions including instructions which, when

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executed by one or more processors, cause the one or more processors to perform the steps of:

receiving integrated circuit layout data that defines a set of two or more layout objects contained in the integrated circuit layout;

performing a first design rule check on a layout object from the set of two or more layout objects by evaluating the layout object against specified design criteria;

changing one or more values defined by the specified design criteria to generate updated specified design criteria, wherein the changing of the one or more values is performed after a specified amount of time has elapsed and is made with respect to either the layout object or one or more other layout objects from the set of two or more layout objects; and

performing a second design rule check on the layout object by evaluating the layout object against the updated specified design criteria.

51. (NEW) A computer-readable medium carrying one or more sequences of one or more instructions for automatically routing an integrated circuit, the one or more sequences of one or more instructions including instructions which, when executed by one or more processors, cause the one or more processors to perform the steps of:

receiving integrated circuit layout data that defines a set of two or more integrated circuit devices to be included in the integrated circuit;

receiving integrated circuit connection data that specifies one or more electrical connections to be made between the integrated circuit devices;

determining, based upon the integrated circuit layout data and the integrated circuit connection data, a set of two or more join points that are to be electrically connected, wherein each join point from the set of two or more

join points has an associated set of specified design criteria that control attachment of routing paths thereto;

determining, based upon the integrated circuit layout data and the set of two or more join points, one or more routing paths to connect the set of two or more join points, wherein the one or more routing paths satisfy the specified design criteria associated with the set of two or more join points; and

updating the integrated circuit layout data to generate updated integrated circuit layout data that reflects the one or more routing paths.

52. (NEW) A computer-readable medium carrying one or more sequences of one or more instructions for automatically routing an integrated circuit, the one or more sequences of one or more instructions including instructions which, when executed by one or more processors, cause the one or more processors to perform the steps of:

receiving integrated circuit layout data that defines a set of two or more integrated circuit devices to be included in the integrated circuit;

receiving integrated circuit connection data that specifies one or more electrical connections to be made between the integrated circuit devices;

determining, based upon the integrated circuit layout data and the integrated circuit connection data, a routing path between first and second integrated circuit devices that satisfies specified design criteria, wherein determining the routing path between the first and second integrated circuit devices includes

determining whether the distance to be routed for a portion of the routing path exceeds a specified distance, and

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if the distance to be routed for the portion of the routing path does not exceed the specified distance, then routing the portion of the routing path in a single step; and

updating the integrated circuit layout data to generate updated integrated circuit layout data that reflects the routing path between the first and second integrated circuit devices.

53. (NEW) The system as recited in Claim 29, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

determining a set of one or more bends to be included in the routing path to avoid the one more obstacles, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the set of one or more bends, the routing path between the first and second integrated circuit devices.

54. (NEW) The system as recited in Claim 29, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

determining one or more portions of the routing path to be ripped up and rerouted, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the one or more portions of the routing path to be ripped up and rerouted, the routing path between the first and second integrated circuit devices.

55. (NEW) The system as recited in Claim 54, wherein determining the routing path between the first and second integrated circuit devices further includes

determining one or more portions of one or more other routing paths to be ripped up and rerouted, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators, the one or more portions of the routing path to be ripped up and rerouted and the one or more portions of the one or more other routing paths to be ripped up and rerouted, the routing path between the first and second integrated circuit devices.

56. (NEW) The system as recited in Claim 29, wherein determining the routing path between the first and second integrated circuit devices further includes

identifying one or more obstacles that block the routing path,

determining one or more portions of one or more other routing paths to be ripped up and rerouted, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the one or more portions of the one or more other routing paths to be ripped up and rerouted, the routing path between the first and second integrated circuit devices.

57. (NEW) The system as recited in Claim 29, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data and the set of one or more routing indicators, the routing

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path between the first and second integrated circuit devices, wherein the routing path is routed from the second integrated circuit device to the first integrated circuit device.

58. (NEW) The system as recited in Claim 29, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

determining one or more locations to employ corner clipping to provide additional space for the routing path, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the one or more locations to employ corner clipping, the routing path between the first and second integrated circuit devices.

59. (NEW) The system as recited in Claim 29, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

determining one or more integrated circuit layout objects to be moved to provide additional space for the routing path, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and moving the one or more integrated circuit layout objects, the routing path between the first and second integrated circuit devices.

60. (NEW) The system as recited in Claim 29, wherein determining the routing path between the first and second integrated circuit devices includes

examining data that indicates whether changes can be made to one or more layout objects defined by the integrated circuit layout data to accommodate the routing of the routing path, and

if the data indicates that changes can be made to the one or more layout objects defined by the integrated circuit layout data to accommodate the routing of the routing path, then

making one or more changes to the one or more layout objects defined by the integrated circuit layout data, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the one or more changes made to the one or more layout objects, the routing path between the first and second integrated circuit devices.

61. (NEW) The system as recited in Claim 60, wherein the routing mechanism is further configured to generate data that specifies the one or more changes made to the one or more layout objects.

62. (NEW) The system as recited in Claim 29, wherein determining the routing path between the first and second integrated circuit devices includes

determining a set of one or more routing targets to which the routing path is to be routed, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the set of one or more routing targets, the routing path between the first and second integrated circuit devices.

63. (NEW) The system as recited in Claim 29, wherein determining the routing path between the first and second integrated circuit devices includes performing one or more design rule checks on one or more portions of the routing path as the routing path is being determined.

64. (NEW) The system as recited in Claim 63, wherein the routing mechanism is further configured to perform a design rule check on the updated integrated circuit layout data, wherein the design rule check does not check one or more layout objects previously checked during determination of the routing path.

65. (NEW) The system as recited in Claim 29, wherein determining the routing path between the first and second integrated circuit devices includes
extending the routing path a specified amount to generate an extended portion of the routing path, and
selectively performing a design rule check on only the extended portion of the routing path.

66. (NEW) The system as recited in Claim 29, wherein all attachment and bend angles defined by the updated integrated circuit layout data are multiples of ninety degrees.

67. (NEW) The system as recited in Claim 29, wherein one or more attachment or bend angles defined by the updated integrated circuit layout data are multiples of other than ninety degrees.